PCI-DAS6402/16

PCI Bus-Compatible Data Acquisition Board

User's Guide

MEASUREMENT COMPUTING™

PCI-DAS6402/16

PCI Bus-Compatible Data Acquisition Board

User's Guide

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Table of Contents

About this User's Guide

What you will learn from this user's guide

This user's guide explains how to install, configure, and use the PCI-DAS6402/16 so that you get the most out of its analog and digital I/O features.

This user's guide also refers you to related documents available on our web site, and to technical support resources.

Conventions in this user's guide

For more information on …

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

<#:#> Angle brackets that enclose numbers separated by a colon signify a range of numbers, such as those assigned to registers, bit settings, etc.

bold text **Bold** text is used for the names of objects on the screen, such as buttons, text boxes, and check boxes. For example:
1. Insert the disk or CD and click the **OK** button.

italic text *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase. For example:
The *Insta*Cal installation procedure is explained in the *Quick Start Guide*.
Never touch the exposed pins or circuit connections on the board.

Where to find more information

Additional information about PCIe-DIO24 hardware is available on our website at www.mccdaq.com. You can also contact Measurement Computing Corporation with specific questions.

- Knowledgebase: kb.mccdaq.com
- Tech support form: www.mccdaq.com/support/support_form.aspx
- Email: techsupport@mccdaq.com
- Phone: 508-946-5100 and follow the instructions for reaching Tech Support

If you need to program at the register level in your application, refer to the *Register Map for the PCIe-DIO24*. This document is available on our website at www.mccdaq.com/registermaps/RegMapPCIe-DIO24.pdf.

Introducing the PCI-DAS6402/16

Overview: PCI-DAS6402/16 features

This manual explains how to install and use the PCI-DAS6402/16.

The PCI-DAS6402/16 is a multifunction measurement and control board designed to operate in computers with PCI bus accessory slots. The architecture of the board is loosely based on the original CIO-DAS16, the standard of ISA bus data acquisition.

The PCI-DAS6402/16 provides the following features:

- 32 differential or 64 single-ended 16-bit analog inputs
- 100-pin high density I/O connector and a 40-pin auxiliary connector
- 200 kHz sample rate
- Two 16-bit analog outputs with update rates of up to 100 kHz
- One 16-bit counter
- 24 DIO bits on the auxiliary connector; four DI bits and 4 DO bits on the 100-pin connector
- Provides arbitrary waveform generation

Analog input ranges are selectable via software as bipolar or unipolar. Bipolar input ranges are ±10 V, ±5 V, ±2.5 V and ±1.25 V. Unipolar input ranges are 0 to 10 V, 0 to 5 V, 0 to 2.5 V and 0 to 1.25 V. The PCI-DAS6402/16 has an analog trigger input. The trigger level and direction are software configurable.

The PCI-DAS6402/16 board is completely plug and play, with no switches, jumpers or potentiometers to set. All board addresses and interrupt sources are set with software.

Software features

For information on the features of *Insta*Cal and the other software included with your PCI-DAS6402/16, refer to the *Quick Start Guide* that shipped with your device. The *Quick Start Guide* is also available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Check www.mccdaq.com/download.htm for the latest software version or versions of the software supported under less commonly used operating systems.

PCI-DAS6402/16 block diagram

PCI-DAS6402/16 functions are illustrated in the block diagram shown here.

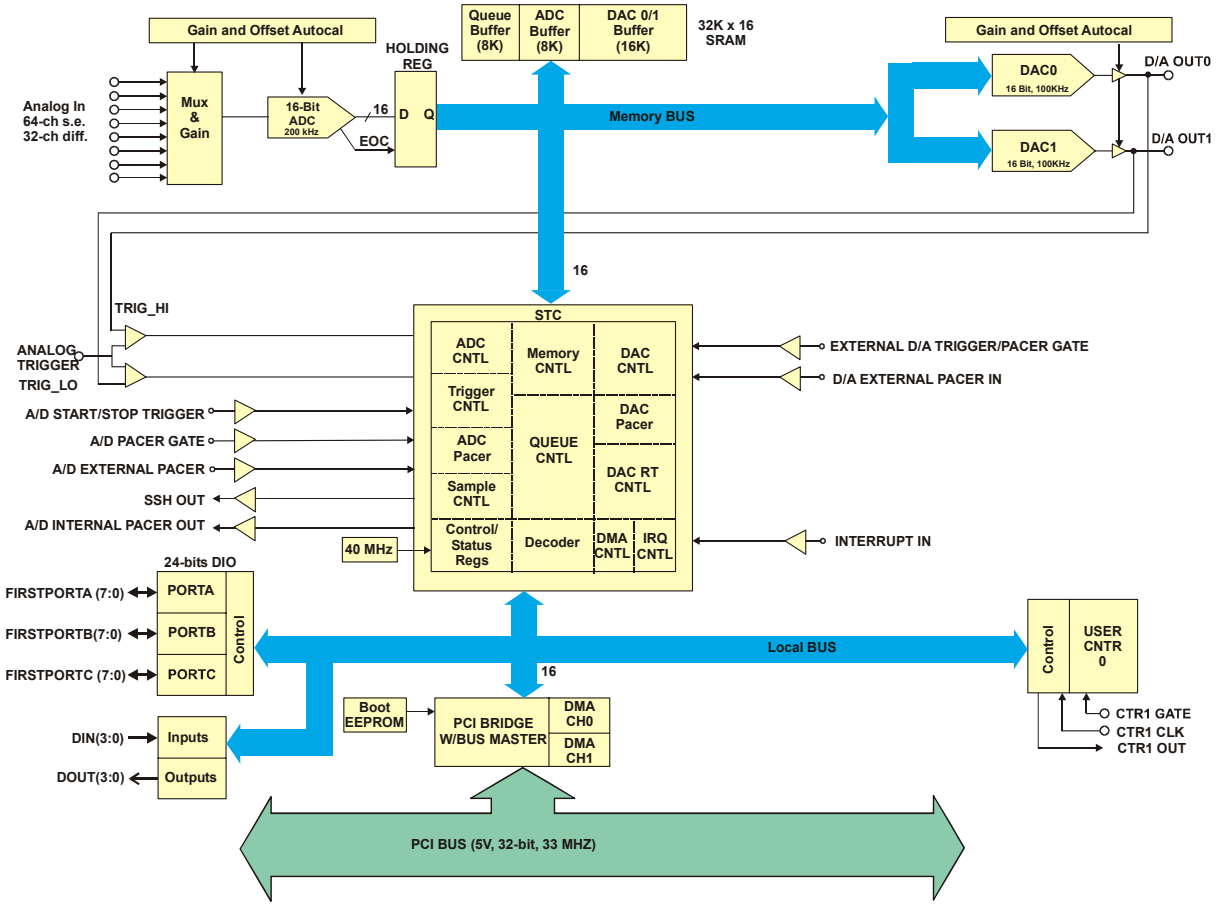

Figure 1-1. PCI-DAS6402/16 functional block diagram

Installing the PCI-DAS6402/16

What comes with your PCI-DAS6402/16 shipment?

The following items are shipped with the PCI-DAS6402/16.

Hardware

- PCI-DAS6402/16

Additional documentation

In addition to this hardware user's guide, you should also receive the *Quick Start Guide* (available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf). This booklet supplies a brief description of the software you received with your PCI-DAS6402/16 and information regarding installation of that software. Please read this booklet completely before installing any software or hardware.

Optional components

If you ordered any of the following products with your board, they should be included with your shipment.

- Cables

C100FF-x

BP40-37-x

C40FF-x

- Signal conditioning accessories

  MCC provides signal termination products for use with the PCI-DAS6402/16. Refer to the "Field wiring, signal termination and conditioning" section on page 2-9 for a complete list of compatible accessory products.

Unpacking the PCI-DAS6402/16

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the PCI-DAS6402/16 from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

If any components are missing or damaged, notify Measurement Computing Corporation immediately by phone, fax, or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

Installing the software

Refer to the *Quick Start Guide* for instructions on installing the software on the *Measurement Computing Data Acquisition Software CD*. This booklet is available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Installing the PCI-DAS6402/16

The PCI-DAS6402/16 board is completely plug-and-play. There are no switches or jumpers to set on the board. Configuration is controlled by your system's BIOS. To install your board, follow the steps below.

Install the MCC DAQ software before you install your board

The driver needed to run your board is installed with the MCC DAQ software. Therefore, you need to install the MCC DAQ software before you install your board. Refer to the *Quick Start Guide* for instructions on installing the software.

1. Turn your computer off, open it up, and insert your board into an available PCI slot.
2. Close your computer and turn it on.

   A dialog box pops up as the system loads indicating that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you will be prompted for the disk containing this file. The MCC DAQ software contains this file. If required, insert the *Measurement Computing Data Acquisition Software* CD and click **OK**.
3. To test your installation and configure your board, run the *Insta*Cal utility you installed in the previous section. Refer to the *Quick Start Guide* that came with your board www.mccdaq.com/PDFmanuals/sm-installation.pdf for information on how to initially set up and load *Insta*Cal.

If your board has been powered-off for more than 10 minutes, allow your computer to warm up for at least 15 minutes before acquiring data. This warm-up period is required in order for the board to achieve its rated accuracy. The high speed components used on the board generate heat, and it takes this amount of time for a board to reach steady state if it has been powered off for a significant amount of time.

Configuring the PCI-DAS6402/16

All of the hardware configuration options on the PCI-DAS6402/16 are software controlled. You can select some of the configuration options using *Insta*Cal, such as the analog input configuration (16 single-ended or eight differential channels), the edge used for triggering when using an external pacer and the source for the two independent counters. Once selected, any program that uses the Universal Library will initialize the hardware according to these selections.

Information on signal connections

General information regarding signal connection and configuration is available in the *Guide to Signal Connections*. This document is available on our web site at www.mccdaq.com/signals/signals.pdf).

Differential input mode

When all channels are configured for differential input mode, 32 analog input channels are available. In this mode, the input signal is measured with respect to the low input. The input signal is typically delivered through three wires:

- The wire carrying the signal to be measured connects to CH# HI.
- The wire carrying the reference signal connects to CH# LO.
- The third wire, typically a system ground, is connected to LLGND.

Differential input mode is the preferred configuration for applications in noisy environments or when the signal source is referenced to a potential other than PC ground.

Single-ended input mode

When all channels are configured for single-ended input mode, 64 analog input channels are available. In this mode, the input signal is referenced to the board's signal ground (LLGND). The input signal is delivered through two wires:

- The wire carrying the signal to be measured connects to CH# IN HI.
- The second wire is connected to LLGND.

Connecting the board for I/O operations

The PCI-DAS6402/16 uses a 100-pin I/O connector (refer to Table 2-2 on page 2-4 and Table 2-3 on page 2-5). The 100-pin connector provides a much greater signal density than the traditional 37-pin connector. Make accurate notes and pay careful attention to wire connections. In a large system, a misplaced wire can create hours of unnecessary troubleshooting.

Connectors, cables – main I/O connector

Table 2-1 lists the board connectors, applicable cables, and compatible accessory products for the PCI-DAS6402/16.

Table 2-1. Board connectors, cables, and compatible hardware

Connector type	▪ Main connector: 100-pin high-density Robinson-Nugent ▪ Auxiliary digital connector: 40-pin header connector
Compatible cable with the main connector	C100FF-x ribbon cable. x = length in feet
Compatible cables with the 40-pin auxiliary connector	C40FF-x cable (x = length in feet)
	C40-37F-x cable (x = length in feet)
	BP40-37 (Translates to a standard CIO-DIO24 type)
Compatible accessory products with the C100FF-x	▪ BNC-16SE ▪ BNC-16DI ▪ CIO-MINI50 ▪ CIO-TERM100 ▪ SCB-50
Compatible accessory products with the C40FF-x	CIO-MINI40
Compatible accessory products with the C40-37F-x cable or with the BP40-37-x and the C37FF-x or C37FFS-x cable	▪ CIO-MINI37 ▪ SCB-37 ▪ CIO-ERB24 ▪ CIO-ERB08 ▪ SSR-RACK24 ▪ SSR-RACK08

Caution! When connecting a cable to the board's I/O connector, make sure that the arrow indicating pin 1 on the board connector lines up with the arrow indicating pin 1 on the cable connector. Incorrectly connected cables can damage the board and the I/O controller.

Pinout – main I/O connector

Table 2-2. . 32-channel differential mode pin out

Signal Name	Pin		Pin	Signal Name
GND	100	• •	50	GND
EXTERNAL INTERRUPT	99	• •	49	SSH OUT/DAC PACER OUT
A/D PACER GATE	98	• •	48	PC +5 V
EXTERNAL D/A TRIGGER/PACER GATE	97	• •	47	A/D STOP TRIGGER IN
D/A EXTERNAL PACER INPUT	96	• •	46	DIN1
A/D INTERNAL PACER OUTPUT	95	• •	45	A/D START TRIGGER IN
DIN3	94	• •	44	DIN0
DIN2	93	• •	43	ANALOG TRIGGER IN
-12 V	92	• •	42	A/D EXTERNAL PACER
GND	91	• •	41	CTR1 OUT
+12 V	90	• •	40	CTR1 GATE
GND	89	• •	39	CTR1 CLK
DOUT3	88	• •	38	D/A OUT 1
DOUT2	87	• •	37	D/A GND 1
DOUT1	86	• •	36	D/A OUT 0
DOUT0	85	• •	35	D/A GND 0
CH31 LO	84	• •	34	CH15 LO
CH31 HI	83	• •	33	CH15 HI
CH30 LO	82	• •	32	CH14 LO
CH30 HI	81	• •	31	CH14 HI
CH29 LO	80	• •	30	CH13 LO
CH29 HI	79	• •	29	CH13 HI
CH28 LO	78	• •	28	CH12 LO
CH28 HI	77	• •	27	CH12 HI
CH27 LO	76	• •	26	CH11 LO
CH27 HI	75	• •	25	CH11 HI
CH26 LO	74	• •	24	CH10 LO
CH26 HI	73	• •	23	CH10 HI
CH25 LO	72	• •	22	CH9 LO
CH25 HI	71	• •	21	CH9 HI
CH24 LO	70	• •	20	CH8 LO
CH24 HI	69	• •	19	CH8 HI
LLGND	68	• •	18	LLGND
CH23 LO	67	• •	17	CH7 LO
CH23 HI	66	• •	16	CH7 HI
CH22 LO	65	• •	15	CH6 LO
CH22 HI	64	• •	14	CH6 HI
CH21 LO	63	• •	13	CH5 LO
CH21 HI	62	• •	12	CH5 HI
CH20 LO	61	• •	11	CH4 LO
CH20 HI	60	• •	10	CH4 HI
CH19 LO	59	• •	9	CH3 LO
CH19 HI	58	• •	8	CH3 HI
CH18 LO	57	• •	7	CH2 LO
CH18 HI	56	• •	6	CH2 HI
CH17 LO	55	• •	5	CH1 LO
CH17 HI	54	• •	4	CH1 HI
CH16 LO	53	• •	3	CH0 LO
CH16 HI	52	• •	2	CH0 HI
LLGND	51	• •	1	LLGND

PCI slot ↓

Table 2-3. 64-channel single-ended mode pin out

Signal Name	Pin		Pin	Signal Name
GND	100	• •	50	GND
EXTERNAL INTERRUPT	99	• •	49	SSH OUT/DAC PACER OUT
A/D PACER GATE	98	• •	48	PC +5 V
EXTERNAL D/A TRIGGER/PACER GATE	97	• •	47	A/D STOP TRIGGER IN
D/A EXTERNAL PACER INPUT	96	• •	46	DIN1
A/D INTERNAL PACER OUTPUT	95	• •	45	A/D START TRIGGER IN
DIN3	94	• •	44	DIN0
DIN2	93	• •	43	ANALOG TRIGGER IN
-12 V	92	• •	42	A/D EXTERNAL PACER
GND	91	• •	41	CTR1 OUT
+12 V	90	• •	40	CTR1 GATE
GND	89	• •	39	CTR1 CLK
DOUT3	88	• •	38	D/A OUT 1
DOUT2	87	• •	37	D/A GND 1
DOUT1	86	• •	36	D/A OUT 0
DOUT0	85	• •	35	D/A GND 0
CH63 IN	84	• •	34	CH47 IN
CH31 IN	83	• •	33	CH15 IN
CH62 IN	82	• •	32	CH46 IN
CH30 IN	81	• •	31	CH14 IN
CH61 IN	80	• •	30	CH45 IN
CH29 IN	79	• •	29	CH13 IN
CH60 IN	78	• •	28	CH44 IN
CH28 IN	77	• •	27	CH12 IN
CH59 IN	76	• •	26	CH43 IN
CH27 IN	75	• •	25	CH11 IN
CH58 IN	74	• •	24	CH42 IN
CH26 IN	73	• •	23	CH10 IN
CH57 IN	72	• •	22	CH41 IN
CH25 IN	71	• •	21	CH9 IN
CH56 IN	70	• •	20	CH40 IN
CH24 IN	69	• •	19	CH8 IN
LLGND	68	• •	18	LLGND
CH55 IN	67	• •	17	CH39 IN
CH23 IN	66	• •	16	CH7 IN
CH54 IN	65	• •	15	CH38 IN
CH22 IN	64	• •	14	CH6 IN
CH53 IN	63	• •	13	CH37 IN
CH21 IN	62	• •	12	CH5 IN
CH52 IN	61	• •	11	CH36 IN
CH20 IN	60	• •	10	CH4 IN
CH51 IN	59	• •	9	CH35 IN
CH19 IN	58	• •	8	CH3 IN
CH50 IN	57	• •	7	CH34 IN
CH18 IN	56	• •	6	CH2 IN
CH49 IN	55	• •	5	CH33 IN
CH17 IN	54	• •	4	CH1 IN
CH48 IN	53	• •	3	CH32 IN
CH16 IN	52	• •	2	CH0 IN
LLGND	51	• •	1	LLGND

PCI slot ↓

Table 2-4. Auxiliary/digital connector pin out

Signal Name	Pin		Pin	Signal Name
NC	40	••	39	NC
NC	38	••	37	DGND
FIRSTPORTA Bit 0	36	••	35	PC +5V
FIRSTPORTA Bit 1	34	••	33	DGND
FIRSTPORTA Bit 2	32	••	31	NC
FIRSTPORTA Bit 3	30	••	29	DGND
FIRSTPORTA Bit 4	28	••	27	NC
FIRSTPORTA Bit 5	26	••	25	DGND
FIRSTPORTA Bit 6	24	••	23	NC
FIRSTPORTA Bit 7	22	••	21	DGND
FIRSTPORTC Bit 0	20	••	19	FIRSTPORTB Bit 0
FIRSTPORTC Bit 1	18	••	17	FIRSTPORTB Bit 1
FIRSTPORTC Bit 2	16	••	15	FIRSTPORTB Bit 2
FIRSTPORTC Bit 3	14	••	13	FIRSTPORTB Bit 3
FIRSTPORTC Bit 4	12	••	11	FIRSTPORTB Bit 4
FIRSTPORTC Bit 5	10	••	9	FIRSTPORTB Bit 5
FIRSTPORTC Bit 6	8	••	7	FIRSTPORTB Bit 6
FIRSTPORTC Bit 7	6	••	5	FIRSTPORTB Bit 7
DGND	4	••	3	NC
PC +5V	2	••	1	NC

Bottom of board ↓

Cabling

Use a C100FF-x 100-pin cable to connect signals to the PCI-DAS6402/16 board. This cable consists of two 50-pin ribbon cables that are joined together at a 100-pin high density header connector (Figure 2-1.)

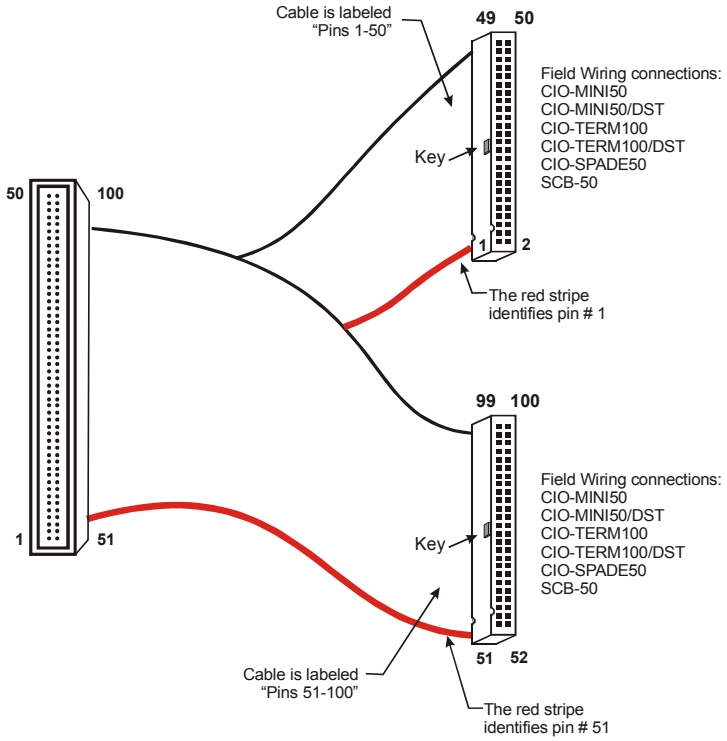

Figure 2-1. C100FF-*x* cable

For signal connections and termination, you can use the CIO-MINI40 screw terminal board and C40FF-x cable. For connections to 37-pin screw terminal boards, you can use the C40-37F-x cable.

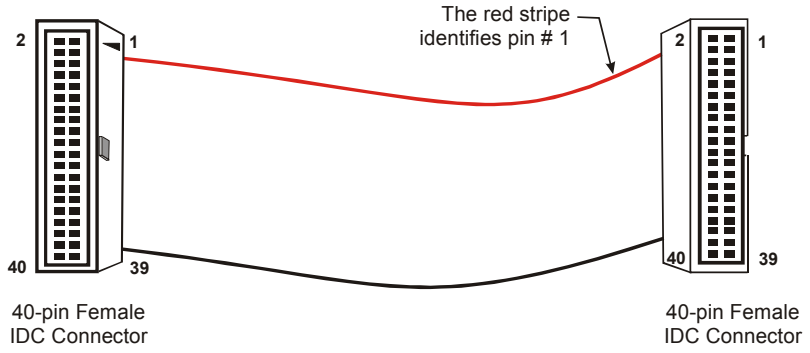

Figure 2-2. C40FF-x cable

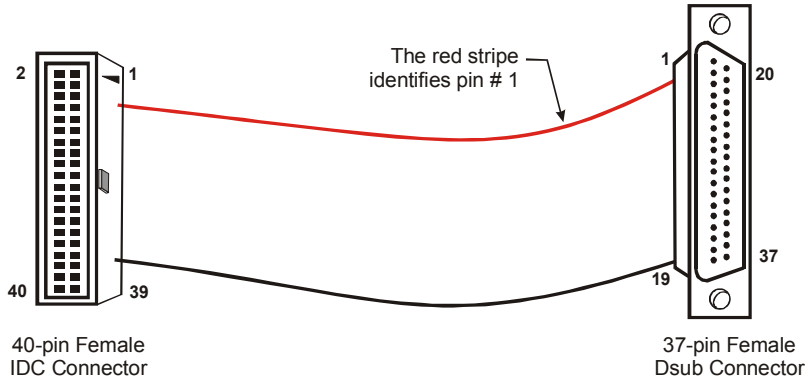

Figure 2-3. C40-37F-x cable

For digital signal conditioning, you can connect the BP40-37 cable to a C37FF-x or C37FFS-x cable, and then connect one of these cables to the 37-pin connector on MCC's digital signal conditioning boards. Refer to page 2-9 for a list of compatible accessories.

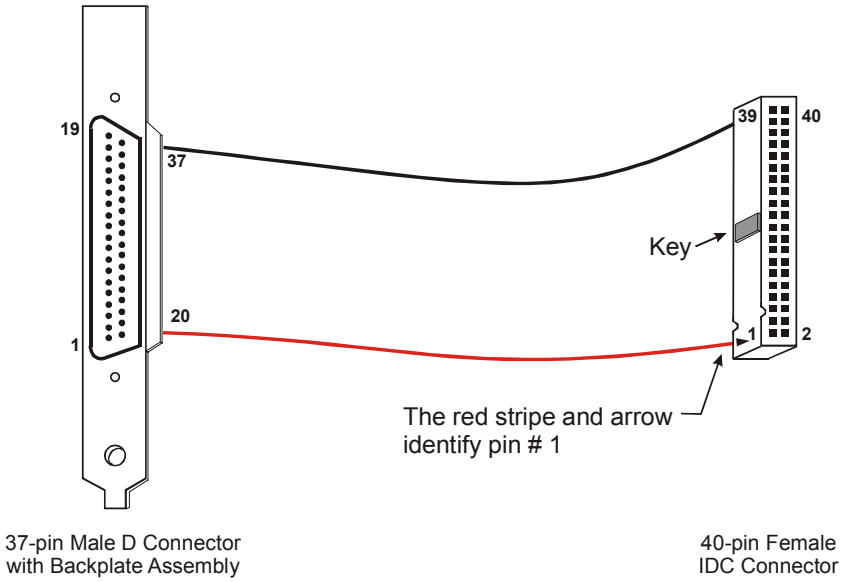

Figure 2-4. BP40-37 cable

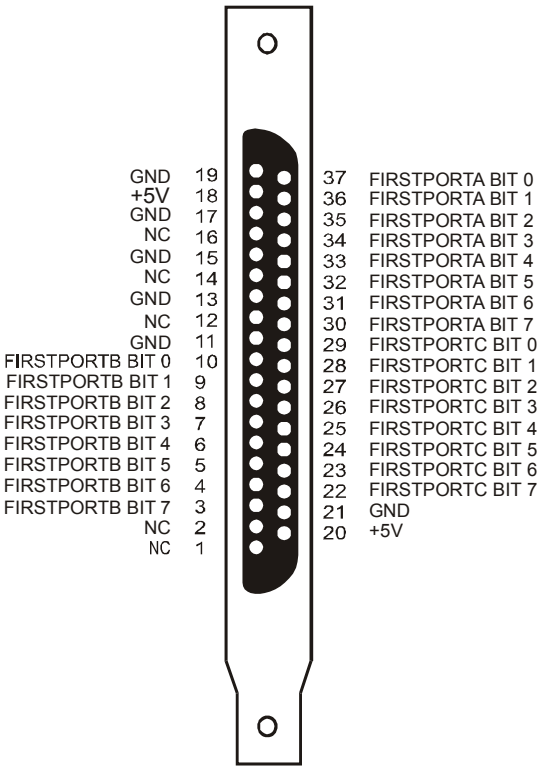

Figure 2-5. BP40-37 cable pin out

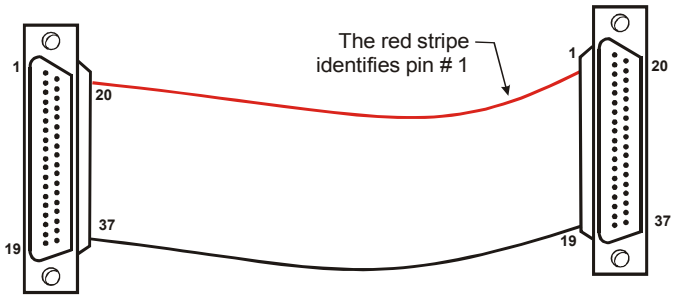

Figure 2-6. C37FF-*x* cable

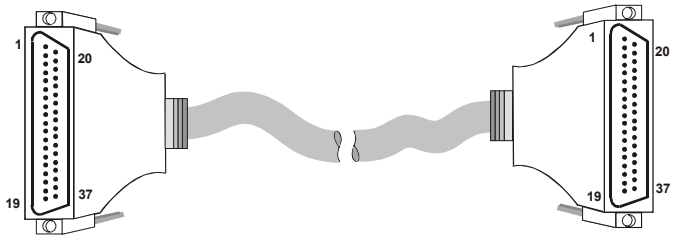

Figure 2-7. C37FFS-*x* cable

40-pin to 37-pin signal mapping

Signal mapping on the C40-37F-x and the BP40-37-x cables is not 1:1. Table 2-5 lists the pin numbers of the signals on the 40-pin end and the pin numbers of the associated signals on the 37-pin end.

Table 2-5. Signal mapping on the C40-37F-x and BP40-37F cables

40-pin cable end		37-pin cable end	
Pin	**Signal Name**	**Pin**	**Signal Name**
1	INTERRUPT IN	1	INTERRUPT IN
2	+5V	20	+5V
3	INTERRUPT ENABLE	2	INTERRUPT ENABLE
4	GND	21	GND
5	Port B 7	3	Port B 7
6	Port C 7	22	Port C 7
7	Port B 6	4	Port B 6
8	Port C 6	23	Port C 6
9	Port B 5	5	Port B 5
10	Port C 5	24	Port C 5
11	Port B 4	6	Port B 4
12	Port C 4	25	Port C 4
13	Port B 3	7	Port B 3
14	Port C 3	26	Port C 3
15	Port B 2	8	Port B 2
16	Port C 2	27	Port C 2
17	Port B 1	9	Port B 1
18	Port C 1	28	Port C 1
19	Port B 0	10	Port B 0
20	Port C 0	29	Port C 0
21	GND	11	GND
22	Port A 7	30	Port A 7
23	N/C	12	N/C
24	Port A 6	31	Port A 6
25	GND	13	GND
26	Port A 5	32	Port A 5
27	N/C	14	N/C
28	Port A 4	33	Port A 4
29	GND	15	GND
30	Port A 3	34	Port A 3
31	N/C	16	N/C
32	Port A 2	35	Port A 2
33	GND	17	GND
34	Port A 1	36	Port A 1
35	+5V	18	+5V
36	Port A 0	37	Port A 0
37	GND	19	GND
38	N/C		
39	N/C		
40	N/C		

Field wiring, signal termination and conditioning

You can use the following MCC screw terminal boards to terminate field signals and route them into the PCI-DAS6402/16 board using the C100FF-x cable:

- **BNC-16SE** – 16-channel single-ended BNC connector box.
- **BNC-16DI** – Eight-channel differential BNC connector box.
- **CIO-MINI50** – 50-pin screw terminal board.
- **CIO-TERM100** – 100 pin, 16 x 4 screw terminal board.
- **SCB-50** – 50-conductor, shielded signal connection box.

You can use the following MCC screw terminal board to terminate field signals and route them into the PCI-DAS6402/16 board using the C40FF-x cable.

- **CIO-MINI40** – 50-pin screw terminal board.

For digital signal conditioning, you can connect the PCI-DAS6402/16 to the following boards using the C40-37F-x cable, or the BP40-37 cable with either the C37FF-x or C37FFS-x cable.

- **SCB-37** – 37-conductor, shielded signal connection/screw terminal box.
- **CIO-MINI37** – 37-pin screw terminal board.
- **CIO-ERB24** – 24 Form C relays, 6 Amp relay accessory board for digital signal conditioning.
- **CIO-ERB08** – Eight Form C relays, 6 Amp relay accessory board for digital signal conditioning.
- **SSR-RACK24** – 24-position solid state relay rack.
- **SSR-RACK08** – Eight-channel solid state relay rack.

Programming and Developing Applications

After following the installation instructions in Chapter 2, your board should now be installed and ready for use. Although the board is part of the larger DAS family, in general there may be no correspondence among registers for different boards. Software written at the register level for other DAS models will not function correctly with your board.

Programming languages

Measurement Computing's Universal Library™ provides access to board functions from a variety of Windows programming languages. If you are planning to write programs, or would like to run the example programs for Visual Basic® or any other language, please refer to the *Universal Library User's Guide* (available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-user-guide.pdf).

Packaged applications programs

Many packaged application programs, such as SoftWIRE®and HP-VEE™, now have drivers for your board. If the package you own does not have drivers for the board, please fax or e-mail the package name and the revision number from the install disks. We will research the package for you and advise how to obtain drivers.

Some application drivers are included with the Universal Library package, but not with the application package. If you have purchased an application package directly from the software vendor, you may need to purchase our Universal Library and drivers. Please contact us by phone, fax or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

Register-level programming

You should use the Universal Library or one of the packaged application programs mentioned above to control your board. Only experienced programmers should try register-level programming. If you need to program at the register level in your application, you can find more information in the *Register Map for the PCI-DAS6402/16 Series* (available at www.mccdaq.com/registermaps/RegMapPCI-DAS6402-16.pdf).

Calibrating the PCI-DAS6402/16

Overview

The PCI-DAS6402/16 provides self-calibration of the analog inputs and outputs, eliminating the need for external equipment and user adjustments. All adjustments are made via 8-bit calibration DACs and digital potentiometers that are referenced to an on-board factory-calibrated standard. The board is fully calibrated at the factory with calibration coefficients stored in nvRAM. At run time, these calibration factors are loaded into system memory and are automatically retrieved each time a different DAC/ADC range is specified.

You can recalibrate any time using factory voltage standards by selecting the **Calibrate** option in *Insta*Cal. A full calibration typically requires less than two minutes. We strongly recommend that you turn your computer on, and allow at least 60 minutes for the internal computer case temperature to stabilize prior to calibrating the board.

Calibration theory

Offset calibration for the analog front end is performed via adjustments of the ADC itself. Front-end gain adjustment is performed only via the ADC reference. This strategy was chosen since the gain tolerance of the in-amp circuit is quite good and there is adequate gain tuning range using only the ADC.

Analog input calibration is shown in Figure 4-1.

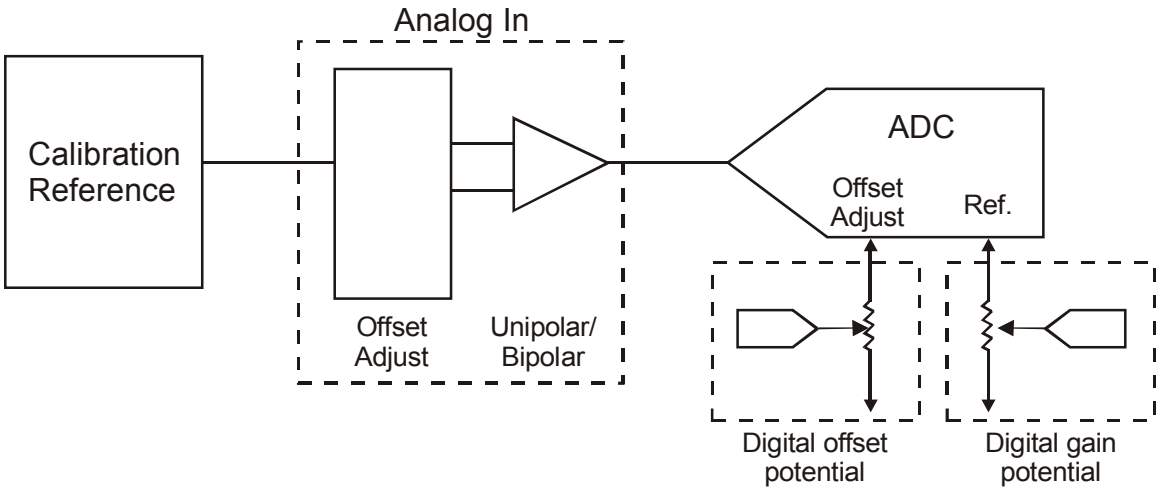

Figure 4-1. Analog input calibration

The analog output circuits are calibrated for gain and offset. Gain calibration of the analog outputs is performed via DAC reference front-end calibration system.

Analog output calibration is shown in Figure 4-2. This circuit is duplicated for both DAC0 and DAC1.

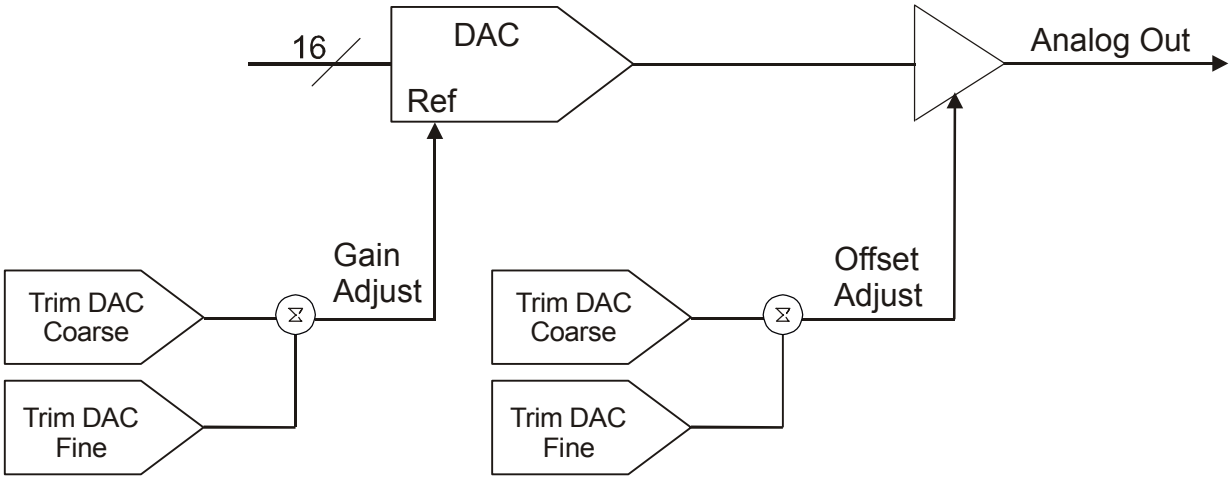

Figure 4-2. Analog output calibration

Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

A/D converter type	AD976A, successive approximation ADC
Resolution	16 bits
Number of channels	64 single ended; 32 differential
Input ranges (SW programmable)	Bipolar: ±10 V, ±5 V, ±2.5 V, ±1.25 V Unipolar: 0 to 10 V, 0 to 5 V, 0 to 2.5 V, 0 to 1.25 V
Polarity	Unipolar/Bipolar, software selectable
A/D pacing (SW programmable)	Internal counter – ASIC
	External source (A/D external pacer)
	Software polled
Burst mode	Software selectable option, burst rate = 5 µS. Valid for a fixed input range only.
A/D gate sources	External digital (A/D Pacer Gate)
	External analog (Analog Trigger In)
A/D gating modes	External digital: Programmable, active high or active low, level, or edge
	External analog: Software-configurable for: ▪ Above or below reference ▪ Positive or negative hysteresis ▪ In or out of window Trigger levels set by D/A OUT 0 and/or D/A OUT 1.
A/D trigger sources	External digital (A/D start trigger in and A/D stop trigger in)
	External analog (analog trigger in)
A/D triggering modes	External digital: Software-configurable for rising or falling edge.
	External analog: Software-configurable for positive or negative slope. Trigger levels set by D/A OUT 0 and/or D/A OUT 1.
	Pre-/post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples. Compatible with both digital and analog trigger options.
Data transfer	From 8k RAM buffer via DMA (demand or non-demand mode) using scatter gather.
	Programmed I/O
Configuration memory	8K words
Channel/gain queue	*Up to 8K elements. Programmable channel, gain, and offset.*
A/D conversion time	5 µS
Calibration	*Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.*

Accuracy

200 kHz sampling rate, single channel operation and a 60 minute warm-up. Accuracies are listed for operational temperatures within ±2 ºC of internal calibration temperature. Calibrator test source high side tied to Channel 0 High and low side tied to Channel 0 Low. Low-level ground is tied to Channel 0 Low at the user connector.

Table 2. Absolute accuracy

Range	Absolute accuracy
±10.000 V	±3.0 LSB
±5.000 V	±3.0 LSB
±2.500 V	±4.5 LSB
±1.250 V	±4.5 LSB
0 V to +10.000 V	±3.0 LSB
0 V to +5.000 V	±3.0 LSB
0 V to +2.500 V	±4.5 LSB
0 V to +1.250 V	±4.5 LSB

Table 3. Accuracy components

Range	Gain error	Offset error	DLE	ILE
±10.00 V	±1.5 max	±1.5 max	±1.75 max	±2 max
±5.000 V	±1.5 max	±1.5 max	±1.75 max	±2 max
±2.500 V	±2.0 max	±2.5 max	±1.75 max	±2 max
±1.250 V	±2.0 max	±2.5 max	±1.75 max	±2 max
0 to +10.00 V	±1.5 max	±1.5 max	±1.75 max	±2 max
0 to +5.000 V	±1.5 max	±1.5 max	±1.75 max	±2 max
0 to +2.500 V	±1.5 max	±3.0 max	±1.75 max	±2 max
0 to +1.250 V	±1.5 max	±3.0 max	±1.75 max	±2 max

Each PCI-DAS6402/16 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in Table 2 above.

As shown in Table 3, total analog input error is a combination of gain, offset, differential linearity and integral linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case errors are realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

System throughput

Table 4. System throughput specifications

Condition	Calibration coefficients	ADC rate (max)
1. Single channel, single input range.	Per specified range	200 kHz
2. Multiple channel, single input range	Per specified range	200 kHz
3. Single channel, multiple input ranges. All samples in unipolar OR bipolar mode.	Default to value for `cbAInScan()` range	200 kHz
4. Multiple channels, multiple input ranges. All samples in unipolar OR bipolar mode.	Default to value for `cbAInScan()` range	200 kHz
5. Multiple channels, multiple input ranges, switching Unipolar/bipolar mode	Default to value for `cbAInScan()` range	200 kHz
6. Multiple channel, single input range, switching Unipolar/bipolar mode.	Default to value for `cbAInScan()` range	200 kHz

Note 1: For conditions 1-2 above, specified accuracy is maintained at rated throughput. Conditions 3-6 apply calibration coefficients which correspond to the range value selected in `cbAInScan()`. These coefficients remain unchanged throughout the scan. Errors of up to 25 counts may be incurred when switching gains while in bipolar or unipolar mode only (conditions 3 and 4). Errors of up to 100 counts may be incurred when mixing unipolar/bipolar modes (conditions 5 and 6).

Crosstalk

Crosstalk is defined here as the influence of one channel upon another when scanning two channels at the maximum rate. A full scale 100 Hz triangle wave is input on Channel 1; Channel 0 is tied to Analog Ground at the 100 pin user connector. The table below summarizes the influence of Channel 1 on Channel 0 with the effects of noise removed. The residue on Channel zero is described in LSBs.

Table 5. Crosstalk specifications

Condition	Crosstalk	Per channel rate	ADC rate
Same range to same range	3 LSB pk-pk	100 kHz	200 kHz
Any range to any range	6 LSB pk-pk	100 kHz	200 kHz

Analog input drift

Table 6. Analog input drift specifications

Analog input full-scale gain drift	0.25 LSB/°C max
Analog input zero drift	0.21 LSB/°C max
Overall analog input drift	0.46 LSB/°C max
Common mode range	±10 V
CMRR @ 60 Hz	-80 dB min
Input impedance	*10 MegOhm min*
Absolute maximum input voltage	▪ *Channel 0: ±15 V, power on or off* ▪ *Channels 1-63: –40 V to +55 V, power on or off*
Warm-up time	60 minutes

Noise performance

Table 7 below summarizes the noise performance for the PCI-DAS6402/16. Noise distribution is determined by gathering 50K samples with inputs tied to ground at the user connector.

Table 7. Board noise performance

Range	Standard Deviation	% within ±2 counts	% within ±1 count	MaxCounts	LSBrms*
±10.00 V	0.8	98%	78%	9	1.4
±5.000 V	0.8	98%	78%	9	1.4
±2.500 V	0.8	98%	78%	9	1.4
±1.250 V	0.9	97%	73%	10	1.5
0 to +10.00 V	0.9	97%	73%	10	1.5
0 to +5.000 V	0.9	97%	73%	10	1.5
0 to +2.500 V	0.9	97%	73%	10	1.5
0 to +1.250 V	1.0	95%	68%	11	1.7

* RMS noise is defined as the peak-to-peak bin spread divided by 6.6

Analog output

Table 8. Analog output specifications

A/D converter type	*AD669BR*
Resolution	*16-bits*
Number of Channels	*2*
Voltage ranges	±10 V, ±5 V, 0 to 10 V, 0 to 5 V. Each channel independently programmable.
Monotonicity	*Guaranteed monotonic over temperature*
Analog output full-scale gain drift	±0.55 LSB/°C
Analog output zero drift	10 V ranges: ±0.25 LSB/°C; 5 V ranges: ±0.45 LSB/°C
Overall analog output drift	10 V ranges: ±0.8 LSB/°C; 5 V ranges: ±1.0 LSB/°C
Slew rate	10 V Ranges: 5 V/µs; 5 V ranges: 2.5 V/µs;
Settling time	20 V step to .0008%:13 µs max; 10 V step to .0008%:6 µs typ
Current drive	±15 mA
Output short-circuit duration	*Indefinite @ 25 mA*
Output coupling	*DC*
Output impedance	0.1 ohms
Power up and reset	DACs cleared to 0 volts ±75 mV max

Accuracy

Table 9. Absolute accuracy specifications

Range	Absolute accuracy
±10.000 V	±4.0 LSB
±5.000 V	±4.0 LSB
0 to +10.000 V	±4.0 LSB
0 to +5.000 V	±4.0 LSB

Table 10. Typical accuracy specifications

Range	Typical accuracy
±10.000 V	±3.5 LSB
±5.000 V	±3.5 LSB
0 to +10.00 V	±3.5 LSB
0 to +5.000 V	±3.5 LSB

Accuracy components

Table 11. Accuracy component specifications

Range	Gain error (LSB)	Offset error (LSB)	DLE (LSB)	ILE (LSB)
±10.000 V	±2.0 max, ±1.5 typ	±2.0 max, ±1.0 typ	±1.0 max, ±0.5 typ	±1.0 max, ±0.5 typ
±5.000 V	±2.0 max, ±1.5 typ	±2.0 max, ±1.0 typ	±1.0 max, ±0.5 typ	±1.0 max, ±0.5 typ
0 to +10.00 V	±2.0 max, ±1.5 typ	±2.0 max, ±1.0 typ	±1.0 max, ±0.5 typ	±1.0 max, ±0.5 typ
0 to +5.000 V	±2.0 max, ±1.5 typ	±2.0 max, ±1.0 typ	±1.0 max, ±0.5 typ	±1.0 max, ±0.5 typ

Each PCI-DAS6402/16 is tested at the factory to assure the board's overall error does not exceed ±4.0 LSB.

Total analog output error is a combination of gain, offset, integral linearity, and differential linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction. Although an examination of the chart and a summation of the maximum theoretical errors shows that the board could theoretically exhibit a ±6.0 LSB error, our testing assures this error is never realized in a board that we ship.

Typical accuracy is derived directly from the various component typical errors. This typical, maximum error calculation for the PCI-DAS6402/16 yields ±3.5 LSB. However, this again assumes that each of the errors contributes in the same direction and the ±3.5 LSB specification is quite conservative.

Analog output pacing and triggering

Table 12. Analog output pacing and triggering specifications

D/A pacing (SW programmable)	Internal counter – ASIC
	External source (D/A external pacer)
	Software paced
D/A gate sources (SW programmable)	▪ External digital (external D/A trigger/pacer gate) ▪ External analog (analog trigger in)
D/A gating modes	▪ External digital: Programmable, active high or active low, level or edge ▪ External analog: Software-configurable for above or below reference. Gating levels set by DAC0 or DAC1
D/A trigger sources	External digital (external D/A trigger/pacer gate)
	Software triggered
D/A triggering modes	External digital: Software-configurable for rising or falling edge.
Data transfer	▪ From 16k RAM buffer via DMA (demand or non-demand mode) using scatter gather. ▪ Programmed I/O ▪ Update DACs individually or simultaneously (SW selectable)
Throughput	100 kHz max per channel, 2 channels simultaneous

Digital input/output

Table 13. Digital input/output specifications (main connector)

Digital type (main connector)	Output: 74LS175
	Input: 74LS244
Configuration	4 inputs, 4 outputs (DIN0 through DIN3; DOUT0 to DOUT3)
Output high voltage (IOH = -0.4 mA)	*2.7 V min*
Output low voltage (IOL = 8 mA)	*0.5 V max*
Input high voltage	*2.0 V min, 7 volts absolute max*
Input low voltage	*0.8 V max, –0.5 volts absolute min*

Table 14. Digital input/output specifications (DIO connector)

Digital type (digital I/O connector)	82C55
Number of I/O	24 (FIRSTPORTA Bit 0 through FIRSTPORTC Bit 7)
Configuration	▪ 2 banks of 8 and 2 banks of 4 or ▪ 3 banks of 8 or ▪ 2 banks of 8 with handshake
Input high voltage	*2.0 V min, 5.5 V absolute max*
Input low voltage	*0.8 V max, –0.5 V absolute min*
Output high voltage (IOH = -2.5 mA)	*3.0 V min*
Output low voltage (IOL = 2.5 mA)	*0.4 V max*
Power-up / reset state	Input mode (high impedance)

Table 15. Simultaneous sample and hold specifications

SSH output	TTL-compatible output, HOLD is asserted from start of the conversion for Channel 0 through conversion of the last channel in the scan. Available at user connector (SSH OUT / D/A PACER OUT). This pin is software selectable as SSH OUT or D/A PACER OUT.
SSH polarity	HOLD high (default) or HOLD low, software selectable

Interrupts

Table 16. Interrupt specifications

Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time	
Interrupt enable	Programmable through PLX9080	
ADC interrupt sources (sw programmable)	DAQ_ACTIVE:	Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP:	Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE:	Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL:	Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE:	Interrupt is generated after each conversion completes.
	DAQ_EOSCAN:	Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ:	Interrupt is generated after each interval delay during multi-channel scans.
DAC interrupt sources (sw programmable)	DAC_ACTIVE:	Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE:	Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY:	Interrupt is generated DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL:	Interrupt is generated when the DAC high channel output is updated.
	DAC_RETRANSMIT:	Interrupt is generated when the end of a waveform sequence has occurred in retransmit mode.
External interrupt	Interrupt is generated via edge-sensitive transition on the External Interrupt pin. Rising/falling edge polarity software selectable.	

Counters

Table 17. Counter specifications

User counter type	82C54
Configuration	One down counter, 16 bits. Counters 2 and 3 not used.
Counter 1 source	External from connector (CTR1 CLK)
Counter 1 gate	Available at connector (CTR1 GATE).
Counter 1 output	Available at connector (CTR1 OUT).
Clock input frequency	*10 MHz max*
High pulse width (clock input)	*30 nS min*
Low pulse width (clock input)	*50 nS min*
Gate width high	*50 nS min*
Gate width low	*50 nS min*
Input low voltage	*0.8 V max*
Input high voltage	*2.0 V min*
Output low voltage	*0.4 V max*
Output high voltage	*3.0 V min*

Pacer

Table 18. Pacer specifications

ADC pacer type	ASIC
Configuration	1 down counter, 24 bits (1 scan interval, 1 sample interval)
ADC pacer Source	40 MHz
ADC pacer Gate	Internally controlled by software/hardware trigger.
ADC pacer Out	ADC pacer clock, available at user connector (A/D pacer out)
DAC Pacer type	ASIC
Configuration	1 down counter, 24 bits (1 scan interval, 1 sample interval)
DAC pacer source	40 MHz or 100 kHz internal source. Software selectable
DAC pacer gate	Internally controlled by software/hardware trigger.
DAC pacer out	DAC pacer clock. Available at connector. (SSH OUT / D/A PACER OUT). This pin is software selectable as SSH OUT or D/A PACER OUT.
Internal pacer crystal oscillator	40 MHz
Frequency accuracy	50 ppm

Power consumption

Table 19. Power consumption specifications

+5 V	2.9A typical, 3.3 max

Environmental

Table 20. Environmental specifications

Operating temperature range	0 to 70 °C
Storage temperature range	-40 to 100 °C
Humidity	0 to 95% non-condensing

Mechanical

Table 21. Mechanical specifications

Card dimensions	312 mm (L) x 100.6 mm (W) x 16 mm (H)

Main connector and pin out

Table 22. Main connector specifications

Connector type	100-pin high-density unshielded Robinson Nugent
Compatible cables	C100FF-x cable (x = length in feet)
Compatible accessory products	BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50

Table 23. 32-channel differential mode pin out

Pin	Signal name	Pin	Signal name
1	LLGND	51	LLGND
2	CH0 HI	52	CH16 HI
3	CH0 LO	53	CH16 LO
4	CH1 HI	54	CH17 HI
5	CH1 LO	55	CH17 LO
6	CH2 HI	56	CH18 HI
7	CH2 LO	57	CH18 LO
8	CH3HI	58	CH19 HI
9	CH3 LO	59	CH19 LO
10	CH4 HI	60	CH20 HI
11	CH4 LO	61	CH20 LO
12	CH5 HI	62	CH21 HI
13	CH5 LO	63	CH21 LO
14	CH6 HI	64	CH22 HI
15	CH6 LO	65	CH22 LO
16	CH7 HI	66	CH23 HI
17	CH7 LO	67	CH23 LO
18	LLGND	68	LLGND
19	CH8 HI	69	CH24 HI
20	CH8 LO	70	CH24 LO
21	CH9 HI	71	CH25 HI
22	CH9 LO	72	CH25 LO
23	CH10 HI	73	CH26 HI
24	CH10 LO	74	CH26 LO
25	CH11 HI	75	CH27 HI
26	CH11 LO	76	CH27 LO
27	CH12 HI	77	CH28 HI
28	CH12 LO	78	CH28 LO
29	CH13 HI	79	CH29 HI
30	CH13 LO	80	CH29 LO
31	CH14 HI	81	CH30 HI
32	CH14 LO	82	CH30 LO
33	CH15 HI	83	CH31 HI
34	CH15 LO	84	CH31 LO
35	D/A GND 0	85	DOUT0
36	D/A OUT 0	86	DOUT1
37	D/A GND 1	87	DOUT2
38	D/A OUT 1	88	DOUT3
39	CTR1 CLK	89	GND
40	CTR1 GATE	90	+12V
41	CTR1 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	ANALOG TRIGGER IN	93	DIN2
44	DIN0	94	DIN3
45	A/D START TRIGGER IN	95	A/D INTERNALPACER OUTPUT
46	DIN1	96	D/A EXTERNAL PACER INPUT
47	A/D STOP TRIGGER IN	97	EXTERNAL D/A TRIGGER/PACER GATE
48	PC +5V	98	A/D PACER GATE
49	SSH OUT / D/A PACER OUT	99	EXTERNAL INTERRUPT
50	GND	100	GND

Table 24. 64-channel single-ended mode pin out

Pin	Signal name	Pin	Signal name
1	LLGND	51	LLGND
2	CH0 IN	52	CH16 IN
3	CH32 IN	53	CH48 IN
4	CH1 IN	54	CH17 IN
5	CH33 IN	55	CH49 IN
6	CH2 IN	56	CH18 IN
7	CH34 IN	57	CH50 IN
8	CH3 IN	58	CH19 IN
9	CH35 IN	59	CH51 IN
10	CH4 IN	60	CH20 IN
11	CH36 IN	61	CH52 IN
12	CH5 IN	62	CH21 IN
13	CH37 IN	63	CH53 IN
14	CH6 IN	64	CH22 IN
15	CH38 IN	65	CH54 IN
16	CH7 IN	66	CH23 IN
17	CH39 IN	67	CH55 IN
18	LLGND	68	LLGND
19	CH8 IN	69	CH24 IN
20	CH40 IN	70	CH56 IN
21	CH9 IN	71	CH25 IN
22	CH41 IN	72	CH57 IN
23	CH10 IN	73	CH26 IN
24	CH42 IN	74	CH58 IN
25	CH11 IN	75	CH27 IN
26	CH43 IN	76	CH59 IN
27	CH12 IN	77	CH28 IN
28	CH44 IN	78	CH60 IN
29	CH13 IN	79	CH29 IN
30	CH45 IN	80	CH61 IN
31	CH14 IN	81	CH30 IN
32	CH46 IN	82	CH62 IN
33	CH15 IN	83	CH31 IN
34	CH47 IN	84	CH63 IN
35	D/A GND 0	85	DOUT0
36	D/A OUT 0	86	DOUT1
37	D/A GND 1	87	DOUT2
38	D/A OUT 1	88	DOUT3
39	CTR1 CLK	89	GND
40	CTR1 GATE	90	+12V
41	CTR1 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	ANALOG TRIGGER IN	93	DIN2
44	DIN0	94	DIN3
45	A/D START TRIGGER IN	95	A/D INTERNALPACER OUTPUT
46	DIN1	96	D/A EXTERNAL PACER INPUT
47	A/D STOP TRIGGER IN	97	EXTERNAL D/A TRIGGER/PACER GATE
48	PC +5V	98	A/D PACER GATE
49	SSH OUT / D/A PACER OUT	99	EXTERNAL INTERRUPT
50	GND	100	GND

Auxiliary DIO connector and pin out

Table 25. DIO connector specifications

Connector type	40-pin header connector
Compatible cables	▪ C40FF-x (x = length in feet) ▪ C40-37F-x (x = length in feet) ▪ BP40-37 (translates to a standard CIO-DIO24 type)
Compatible accessory products with the C40FF-x cable	CIO-MINI40
Compatible accessory products with the C40-37F-x cable or with the BP40-37 and the C37FF-x or C37FFS-x cable	CIO-MINI37 SCB-37 CIO-ERB24 CIO-ERB08 SSR-RACK24 SSR-RACK08

Table 26. Digital I/O connector pin out

Pin	Signal name	Pin	Signal name
1	NC	2	PC +5V
3	NC	4	DGND
5	FIRSTPORTB Bit 7	6	FIRSTPORTC Bit 7
7	FIRSTPORTB Bit 6	8	FIRSTPORTC Bit 6
9	FIRSTPORTB Bit 5	10	FIRSTPORTC Bit 5
11	FIRSTPORTB Bit 4	12	FIRSTPORTC Bit 4
13	FIRSTPORTB Bit 3	14	FIRSTPORTC Bit 3
15	FIRSTPORTB Bit 2	16	FIRSTPORTC Bit 2
17	FIRSTPORTB Bit 1	18	FIRSTPORTC Bit 1
19	FIRSTPORTB Bit 0	20	FIRSTPORTC Bit 0
21	DGND	22	FIRSTPORTA Bit 7
23	NC	24	FIRSTPORTA Bit 6
25	DGND	26	FIRSTPORTA Bit 5
27	NC	28	FIRSTPORTA Bit 4
29	DGND	30	FIRSTPORTA Bit 3
31	NC	32	FIRSTPORTA Bit 2
33	DGND	34	FIRSTPORTA Bit 1
35	PC +5V	36	FIRSTPORTA Bit 0
37	DGND	38	NC
39	NC	40	NC

CE Declaration of Conformity

Manufacturer: Measurement Computing Corporation
Address: 10 Commerce Way
Suite 1008
Norton, MA 02766
USA

Category: Electrical equipment for measurement, control and laboratory use.

Measurement Computing Corporation declares under sole responsibility that the product

PCI-DAS6402/16

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EU EMC Directive 89/336/EEC: Electromagnetic Compatibility, EN55022 (1995), EN55024 (1998)

Emissions: Group 1, Class B

- EN55022 (1995): Radiated and Conducted emissions.

Immunity: EN55024

- EN61000-4-2 (1995): Electrostatic Discharge immunity, Criteria A.
- EN61000-4-3 (1997): Radiated Electromagnetic Field immunity Criteria A.
- EN61000-4-4 (1995): Electric Fast Transient Burst immunity Criteria A.
- EN61000-4-5 (1995): Surge immunity Criteria A.
- EN61000-4-6 (1996): Radio Frequency Common Mode immunity Criteria A.
- EN61000-4-8 (1994): Power Frequency Magnetic Field immunity Criteria A.
- EN61000-4-11 (1994): Voltage Dip and Interrupt immunity Criteria A.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in September, 2001. Test records are outlined in Chomerics Test Report #EMI3053.01.

We hereby declare that the equipment specified conforms to the above Directives and Standards.

Carl Haapaoja, Director of Quality Assurance

Measurement Computing Corporation
10 Commerce Way
Suite 1008
Norton, Massachusetts 02766
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@mccdaq.com
www.mccdaq.com